STD 7000

7815

8085A Processor Card

USER'S MANUAL

FOREWORD

This manual explains how to use the Pro-Log 7815 Processor Card. It is structured to reflect the answers to basic questions you might ask yourself about the 7815. We welcome your suggestions on how we can improve our instructions.

The 7815 is part of the Pro-Log Series 7000 STD BUS hardware. Our products are modular, and designed and built with second-sourced parts that are industry standards. They provide industrial managers with the means of using their own people to control the design, production, and maintenance of the products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, we teach courses on how to design with and use microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: the Microprocessor User's Guide and the Series 7000 STD BUS Technical Manual. If you would like a copy of these documents, please write to us on your company letterhead.

CONTENTS

	Page
Foreword	ii
Figures	iv
References/Bibliography	v
Section 1. Purpose and Main Features	1-1
Purpose	1-1
Features	1-1
Functional Description	1-2
Section 2. Installation and Specifications	2-1
Introduction	2-1
Installation	2-1
Jumpers	2-2
Memory Mapping	2-5
Memory Devices	2-5
MEMEX and Segment	2-6
Onboard Port	2-7
Interrupt Jumper	2-7
User Connectors (J1 and J2)	2-8
IOEXP	2-8
Timing Specifications	2-9
Electrical and Environmental Specifications	2-14
Power-On and Pushbutton Reset	2-15
Cabling	2-15
Mechanical Specifications	2-15
Section 3. Operation and Programming	3-1
Introduction	3-1
Power-On and Pushbutton Reset Circuit	3-1
MEMEX and Segment Control	3-2
Section 4. Operating Software	4-1
MEMEX Control Software Example	4-1
Section 5. Maintenance	5-1
Reference Drawings	5-1
Return for Repair/Warranty	5-5

FIGURES

Figure		Page
1-1	7815 Processor Card	1-1
1-2	Block Diagram (7815)	1-2
2-1	Installation in STD BUS Card Rack	2-1
2-2	Jumper Locations	2-2
2-3	Jumper Functions	2-3
2-4	Memory Mapping and Type	2-4
2-5	MEMEX Affecting Onboard Memory	2-5
2-6	MEMEX Port Configuration	2-5
2-7	Segment Port Configuration	2-6
2-8	Onboard Port Configuration	2-6
2-9	Load Characteristics & Pinouts, J1 & J2 Connectors	2-7
2-10	Reset After Power-Up	2-8
2-11	Read Timing: Memory Read, Input and Interrupt	2-9
2-12	Write Timing: Memory Write and Output	2-10
2-13	Wait Request Timing	2-11
2-14	Bus Request Timing	2-12
2-15	Electrical Specifications	2-13
2-16	Electrical Characteristics	2-13
2-17	Environmental Specifications	2-13
2-18	STD BUS Edge Connector Pin List	2-15
3-1	Reset Circuit	3-1
3-2	MEMEX Example in a 96K System	3-3
3-3	MEMEX Example in a 128K System	3-4
4-1	MEMEX Control Software Example Diagram	4-2
4-2	MEMEX Control Software Example Flowchart	4-3
4-3	MEMEX Control Software Program Listing	4-4
5-1	Schematic (Reference Only)	5-2
5-2	Schematic (Reference Only)	5-3
5-3	Assembly Drawing (Reference Only)	5-4

Series 7000 STD BUS Technical Manual, Monterey, CA: Pro-Log Corporation.

1983 Microprocessor and Peripheral Handbook, Santa Clara, CA: Intel Corporation, 210844: pps 2-10 through 2-25.

1979 MCS-80/85 Family User's Manual, Santa Clara, CA: Intel Corporation, 121506-001.

PURPOSE

The 7815 processor card combines a buffered and fully expandable 8085A microprocessor with four 8K-byte memory sockets. Each socket accepts EPROM parts or CMOS RAM.

An input and an output connector are provided to access the 7.5, 6.5, and 5.5 interrupt pins, the serial input data (SID) and serial output data (SOD) pins, and a programmable Segment select (SGMT) pin.

The 7815 is available in two clock speeds:

7815-1: 6.144 MHz crystal producing 325.5 ns ±0.05% time states
7815-0: 6.250 MHz crystal producing 320 ns ±0.05% time states

The 7815 responds to the STD BUS signal BUSRQ* allowing direct memory access (DMA) to other cards in the system.

FEATURES

- 8085A processor
- 32K-byte capacity, four 8K by 8 RAM/EPROM memory sockets
- DMA to onboard memory sockets
- 6.144 and 6.250 MHz crystal
- User connections for 8085A interrupts, SID, and SOD
- Advanced power-on reset circuit with Vcc sensing
- MEMEX and Segment select (SGMT) memory expansion control
- Single +5V operation
- Gold-plated connectors and jumper posts

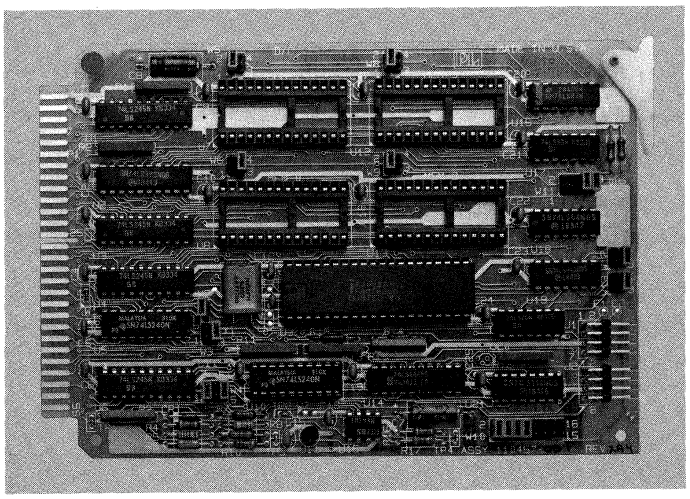


Figure 1-1. Processor Card (7815)

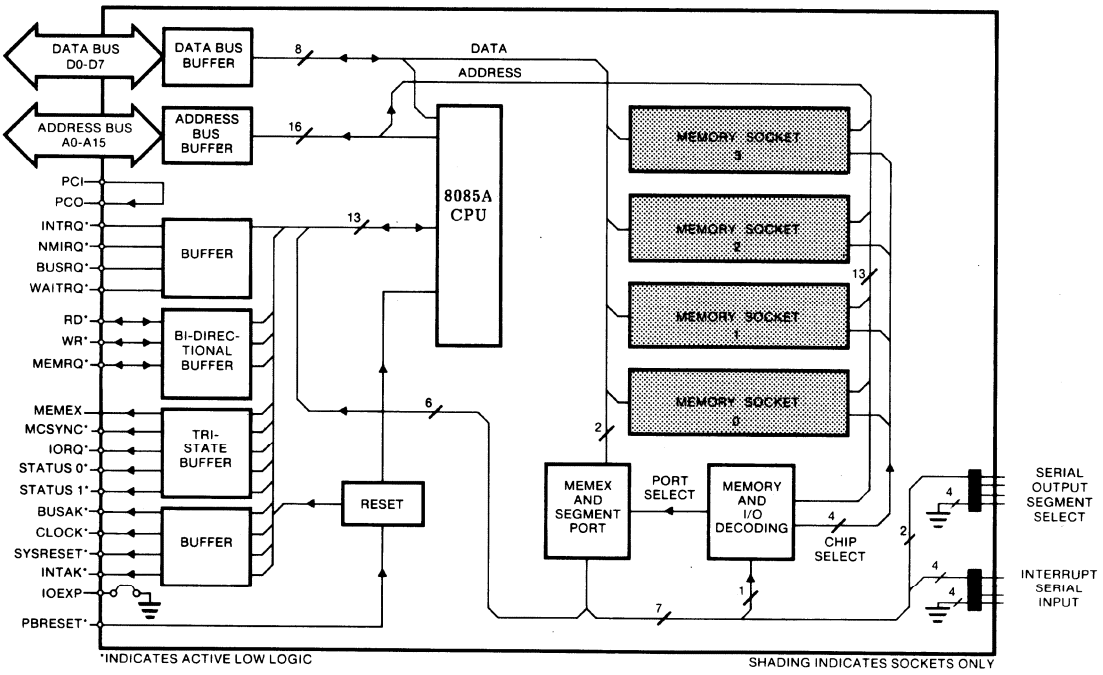


Figure 1-2. Block Diagram (7815)

FUNCTIONAL DESCRIPTION

This portion of section 1 describes the function of each block of circuitry shown in the functional block diagram of figure 1-2.

8085A CPU — The 8085A CPU is one of the industry standard 8-bit microprocessors. This CPU has four vectored interrupt inputs one of which is nonmaskable, serial input and serial output ports, and direct addressing to 64K bytes of memory.

ONBOARD MEMORY — The onboard memory consists of four 28-pin sockets. This memory can be up to 32K bytes in any combination of four 8K by 8 RAMs or ROMs.

MEMORY DECODE — The memory decode consists of a 3 to 8 memory decoder. This circuitry decodes the memory address lines into 8K blocks to select the addressed memory socket. For more information, see section 2, Installation and Specifications.

I/O DECODE — The I/O decode section selects the onboard port and decodes the address lines only during an I/O write cycle. MEMEX and Segment can be written through the onboard port.

RESET — The reset circuit resets the CPU during power-up or during a pushbutton reset. During power-up, the circuit keeps the CPU in a reset state until the power supply reaches a voltage in the proper operating range. This delay ensures that the CPU has a valid power supply when it leaves reset, which prevents latch-up. The pushbutton reset circuit debounces the pushbutton input.

MEMEX AND SEGMENT PORT — Both the STD BUS memory expansion line, MEMEX, and the user card edge memory expansion line, Segment, are controlled by the on-card port of the 7815. Both signals provide control to expand memory for large systems. See section 3, Operation and Programming, for more detail.

Section 2

INSTALLATION AND SPECIFICATIONS

INTRODUCTION

This section covers all aspects of the 7815 to review before operation, including installation, jumper-selected optional functions, and cabling. Complete specifications for the 7815 are included at the end of this section.

INSTALLATION

> **CAUTION**
>
> TO PREVENT POSSIBLE DAMAGE TO YOUR STD BUS SYSTEM, MAKE SURE THAT POWER IS **OFF** BEFORE INSERTING A CARD INTO THE RACK OR BEFORE REMOVING A CARD FROM THE RACK.

The 7815 can operate independently or as part of an STD BUS system. The card should be installed in an STD BUS backplane or card rack with the card ejector toward the top, as shown in figure 2-1. The card can be installed into any slot in the rack.

To access the card for testing or servicing, a card extender such as the Pro-Log 7901 may be used.

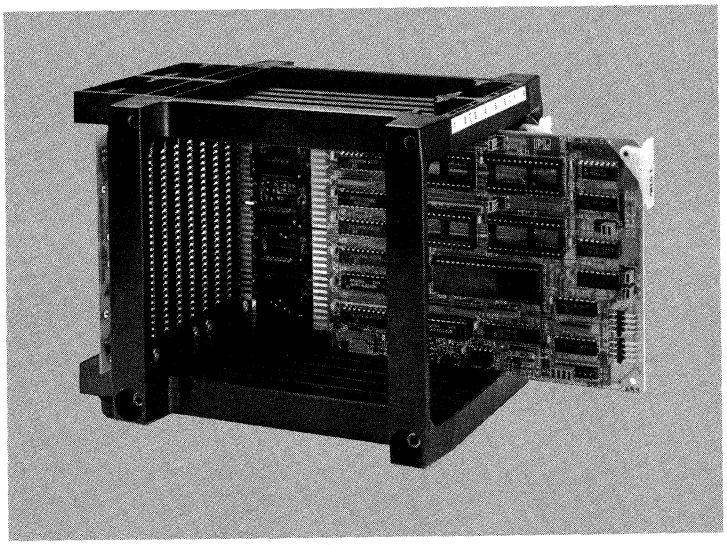


Figure 2-1. Installation in STD BUS Card Rack

JUMPERS

There are several optional functions on the 7815 which are selected by jumpers. Most of the jumpers are wirewrap posts which can be shorted by supplied shorting plugs (Elco Corporation, part number 00 8261 02 42 00 870) or by wire wrapping. Some of the card jumpers are soldered wire. To disconnect these, cut each wire jumper in two places to prevent reshorting. When removing wire jumpers, be sure to cut them and remove one half at a time to prevent circuit trace damage. The wire jumpers can be replaced with a pair of wirewrap posts (Elco Corporation, part number 00 8261 02 32 00 852). Figure 2-2 shows the jumper locations and figure 2-3 lists their functions. Review the jumper options available and check to be certain the card is properly configured to your specific application before installing it in the system.

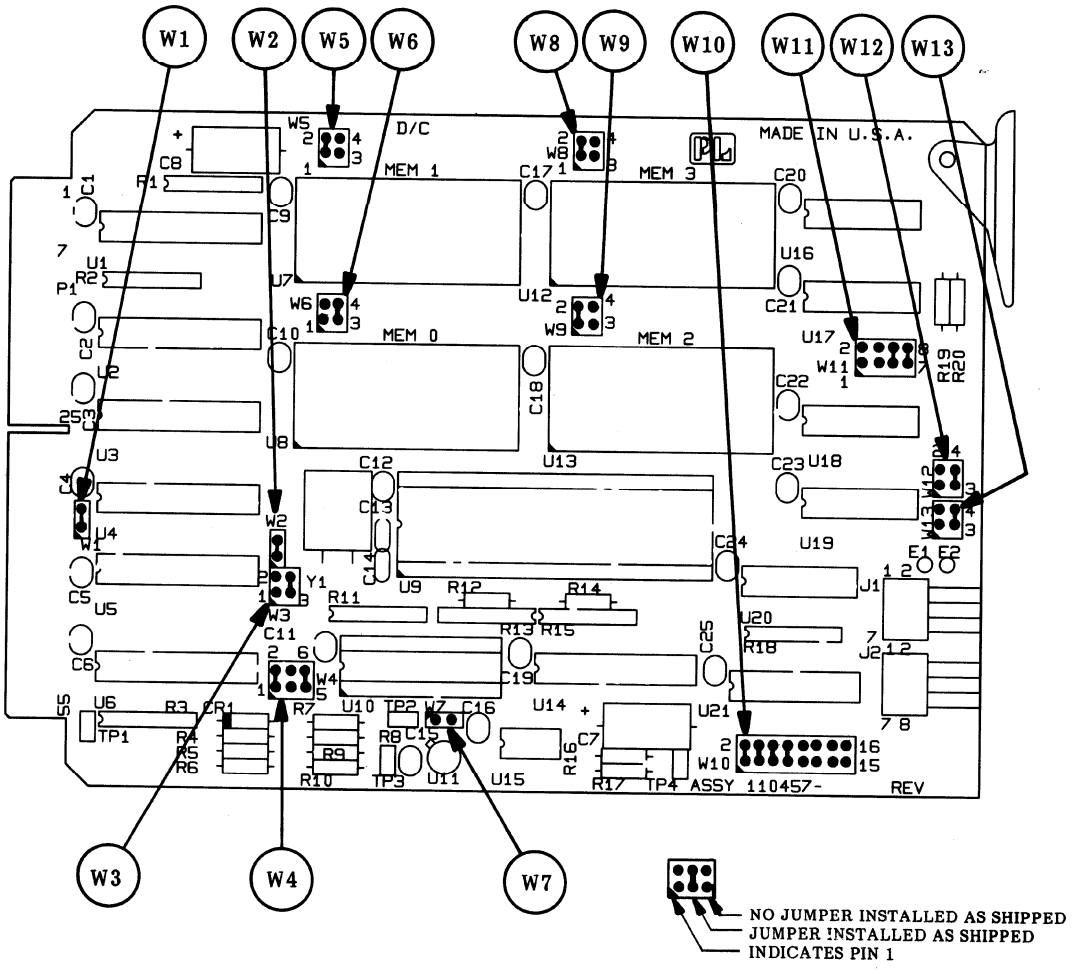


Figure 2-2. Jumper Locations (7815)

JUMPER	PINS	DESCRIPTION	JUMPER INSTALLED AS SHIPPED
W1	1-2 no jumper	IOEXP is connected to ground. IOEXP must be controlled by another card.	1-2
W2	1-2 no jumper	The 78C15 controls MEMEX. MEMEX must be controlled by another card.	1-2
W3	1-2 3-4 no jumper	On-card memory responds to MEMEX high if enabled. On-card memory responds to MEMEX low if enabled. On-card memory is independent of MEMEX.	3-4
W4	1-2 3-4 5-6	Connects the J2-8 RS5.5* pin to the RST5.5 8085 input. Connects the STD INTRQ* signal to the RST5.5 8085 input. Connects the STD INTRQ* signal to the 8085 INTR (interrupt) input.	1-2,5-6
W6, W5, W9, W8	1-2 3-4	Configures the memory socket (MEM 0 - MEM 3 respectively) for a 28-pin 8K x 8 RAM device. Configures the memory socket for 28-pin 8K x 8 ROM or EPROM.	3-4 MEM 0 1-2 MEM 1 1-2 MEM 2 1-2 MEM 3
W7	no jumper	For Pro-Log use only	no jumper
W10	no jumper 1-2 thru 7-8 9-10 thru 15-16	Disables all onboard memory. Enables memory sockets (MEM 0-3 respectively) in the lower 32K address range (0000_H-$7FFF_H$). Enables memory sockets (MEM0-3 respectively) in the upper 32K address range (8000_H-$FFFF_H$).	1-2 thru 7-8
W11	1-2, 3-4 5-6,7-8 no jumper	MEMEX and Segment control port address is 7F. MEMEX and Segment control port address is FE. Control port is disabled	5-6,7-8
W12	1-2 3-4	Segment is low at power-up and its port is noninverting. Segment is high at power-up and its port is inverting.	3-4
W13	1-2 3-4	MEMEX is high at power-up, and its port is inverting. MEMEX is low at power-up, and its port is noninverting.	3-4

Figure 2-3. Jumper Functions (7815)

MEMORY MAPPING (W5, W6, W8, W9, W10)

The 7815 processor card contains four 28-pin sockets for 8K by 8 CMOS byte-wide memories. Using the W10 jumpers, the 7815 memory sockets can be mapped to either the upper or lower 32K address space and can be enabled (jumper in) or disabled (jumper out) on 8K boundaries. The card can be mapped as shown in figure 2-4 with the W10 jumpers. Unused sockets on the card can be disabled for off-card use by removing the appropriate W10 jumper.

		W10			
CHIP REF.	MEMORY SOCKET	UPPER ADDRESS	LOWER ADDRESS		TYPE
U8	MEM 0	pins 9-10 8000-9FFF	pins 1-2 0000-1FFF	W6	1-2 RAM 3-4 EPROM (as shipped)
U7	MEM 1	pins 11-12 A000-BFFF	pins 3-4 2000-3FFF	W5	1-2 RAM (as shipped) 3-4 EPROM
U13	MEM 2	pins 13-14 C000-DFFF	pins 5-6 4000-5FFF	W9	1-2 RAM (as shipped) 3-4 EPROM
U12	MEM 3	pins 15-16 E000-FFFF	pins 7-8 6000-7FFF	W8	1-2 RAM (as shipped) 3-4 EPROM

Figure 2-4. Memory Mapping and Type

MEMORY DEVICES

The 7815 processor card uses byte-wide memory components that are compatible with the 28-pin JEDEC standard. For example, two memory devices which are acceptable are the Hitachi HM6264-15 8Kx8 CMOS and the Intel 2764-2 8Kx8 EPROM. To use other memory components, compare the manufacturer's data sheets to the socket configurations and check for any special requirements.

One of the most critical requirements is the access timings. Timings for all memories used with the 7815 should be less than or equal to the limits specified below.

t_{ACC}	Address to Output Delay	550 ns	MAX
t_{CE}	Chip enable to Output Delay	525 ns	MAX
t_{OE}	Output enable to Output Delay	295 ns	MAX

MEMEX AND SEGMENT (W3, W13, W2, W12)

MEMEX and Segment are both controls for expanded memory schemes. For more detailed information, see section 3, Operation and Programming.

Several jumpers affect MEMEX. **W3** determines how MEMEX affects onboard memory. Figure 2-5 shows the position of W3 in relation to MEMEX. If no pins of W3 are jumpered, the onboard memory is permanently enabled regardless of the state of MEMEX.

W3 JUMPER POSITION	ONBOARD MEMORY ENABLED WHEN
1-2	MEMEX high
3-4*	MEMEX low
No Jumpers	Always Enabled

* As shipped configuration

Figure 2-5. MEMEX Affecting Onboard Memory

Jumper **W13** determines the state of MEMEX after reset (when controlled by the 7815) and whether the data written to the MEMEX port is to be inverted. Figure 2-6 shows the possible configurations.

W13 PIN NUMBER	STATE AFTER RESET	DATA FROM PORT
1-2	MEMEX high	inverted
3-4*	MEMEX low	noninverted

* As shipped configuration

Figure 2-6. MEMEX Port Configuration

Jumper **W2** determines which card controls MEMEX. With the jumper installed MEMEX is controlled by the 7815. Otherwise MEMEX is left floating to be controlled by another card.

W12 determines the state of Segment after reset and whether the data written to the Segment port is to be inverted. Figure 2-7 shows the possible configurations.

W12 PIN NUMBER	STATE AFTER RESET	DATA FROM PORT
1-2	Segment low	noninverted
3-4*	Segment high	inverted

* As shipped condition

Figure 2-7. Segment Port Configuration

ONBOARD PORT (W11)

Jumper **W11** affects the configuration of the onboard port through which data for MEMEX and Segment are passed. Jumper W11 determines the address of the port. Figure 2-8 shows the possible configurations.

W11 PIN NUMBERS	PORT ADDRESS
1-2, 3-4	Port 7F
5-6*, 7-8*	Port FE
No Jumpers	Port Disabled

* As shipped configuration

Figure 2-8. Onboard Port Configuration

INTERRUPT JUMPER (W4)

Jumper **W4** gives the user flexibility when using the 8085A interrupts. Pins 1 and 2 connect the RS5.5* signal (user edge connector J2, pin 8) to the 8085A RST5.5 input (pin 9). Jumper positions 3-4 and 5-6 determine the type of processor interrupt caused by the STD BUS INTRQ* signal. Jumper position 3-4 connects INTRQ* to the 8085A RST5.5 input so the interrupt address is $002C_H$. Jumper position 5-6 connects INTRQ* to the 8085A INTR input (pin 10) so the interrupt routine address **must be** available to the CPU on the data lines during interrupt acknowledge. When using this option, an interrupt controller card which supplies an interrupt address vector should be used. As an alternative, the STD data lines are pulled up with resistor networks R1 and R2 which provide an FF interrupt vector address to the 8085A.

NOTE: To prevent erroneous interrupts, W4 should be configured to either pins 1-2 and 5-6 or 3-4 only.

USER CONNECTORS

The J1 and J2 connectors allow user access to several pins on the 8085A chip in addition to a general output line (SGMT). The J1 connector pins are outputs only: The J2 pins are inputs only. Each signal pin is paired with a ground pin for use with twisted pair interconnect cables such as the Pro-Log RC704-1 and RC704-2 cables.

The J1 connector contains a digital output line (SGMT, pin 6), a serial output data line (SOD, pin 8), and two spare lines with PCB pads (pins 2 and 4). The J2 connector contains the serial input data line (SID*, pin 2) and the 8085A vectored interrupt lines: RS7.5*, RS6.5*, and RS5.5* (pins 4, 6, and 8 respectively).

J1 (OUTPUT) and J2 (INPUT) PIN LOADING

	MNEMONIC	PIN NUMBER OUTPUT (LSTTL LOADS)#	INPUT (LSTTL LOADS)#	PIN NUMBER	PIN NUMBER	OUTPUT (LSTTL LOADS)	INPUT (LSTTL LOADS)	MNEMONIC
	Spare			2	1	OUT		Ground
	Spare			4	3	OUT		Ground
J1	SGMT		55	6	5	OUT		Ground
	SOD*		55	8	7	OUT		Ground
	SID*	3		2	1		IN	Ground
	RS7.5*	3		4	3		IN	Ground
J2	RS6.5*	3		6	5		IN	Ground
	RS5.5*	3		8	7		IN	Ground

* Designates active low- level logic

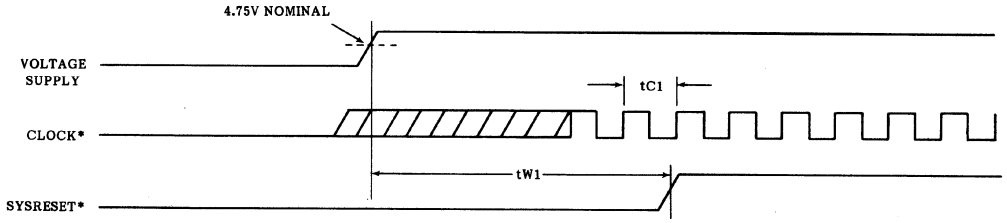
Figure 2-9. Load Characteristics & Pinouts for J1 and J2 Connectors

IOEXP (W1)

IOEXP is one of the STD BUS standard signals. IOEXP enables or expands I/O port addressing. Jumper W1 determines which card controls the IOEXP line. With the jumper installed, IOEXP is grounded by the 7815. With no jumper, IOEXP is left floating to be controlled by another card.

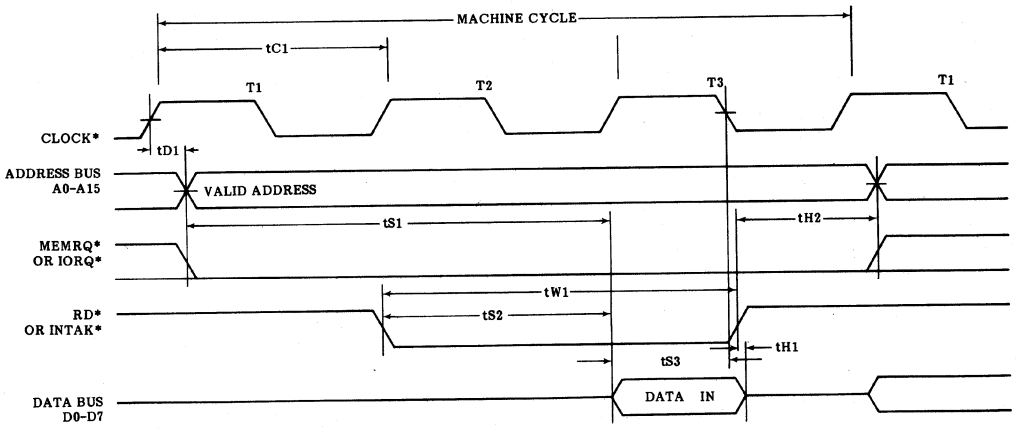
TIMING SPECIFICATIONS

Figures 2-10 through 2-14, pages 2-8 through 2-12, show the signal sequences and timing for various 7815 functions. These signals are shown as they appear at the card edge connector of the 7815.



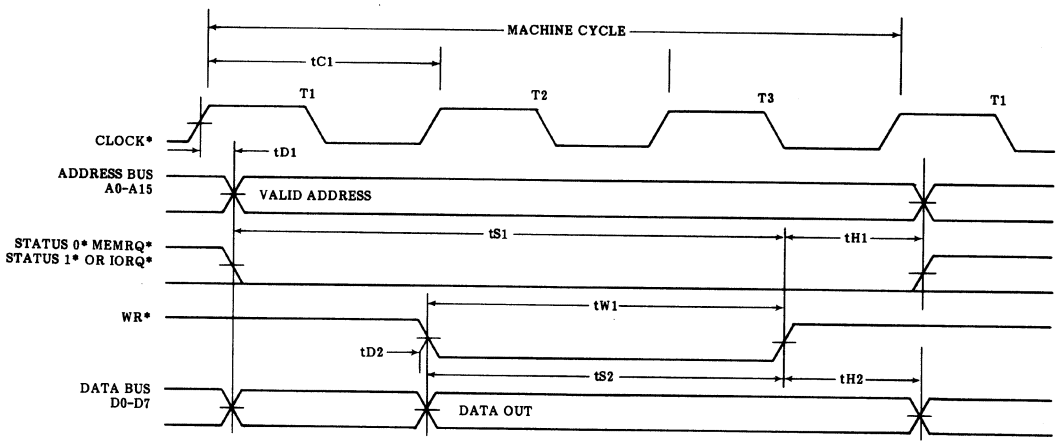
SYMBOL	PARAMETER	UNIT	6.250 MHz MIN	6.250 MHz MAX
tC1	Clock cycle time	ns		320
tW1	Power-up reset width after supply threshold	ms	10	2?60

Figure 2-10. Reset After Power-Up (7815)



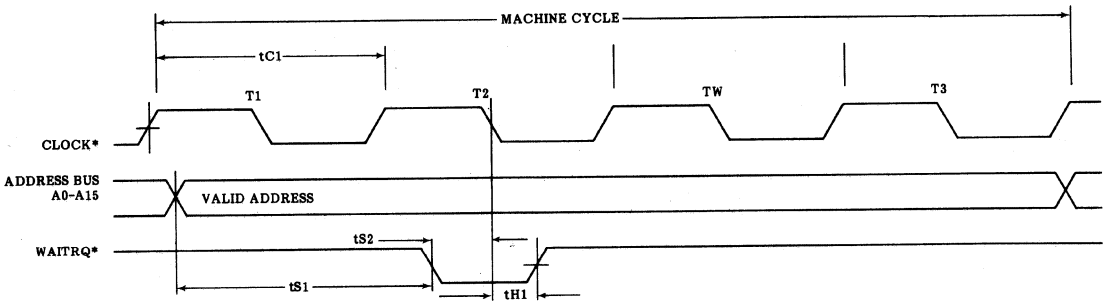
SYMBOL	PARAMETER	UNIT	6.250 MHz		6.144 MHz	
			MIN	MAX	MIN	MAX
tC1	Clock cycle time	ns		320		325
tD1	Address delay from T1 clock	ns		135		135
tH1	Data hold time	ns	0		0	
tH2	Hold time after RD*	ns	110		110	
tS1	Address setup before data valid	ns		410		420
tS2	RD* setup before data valid	ns		270		280
tS3	Data setup time	ns	125		125	
tW1	RD* pulse width	ns	385		390	

Figure 2-11. Read Timing: Memory Read, Input, and Interrupt (7815)



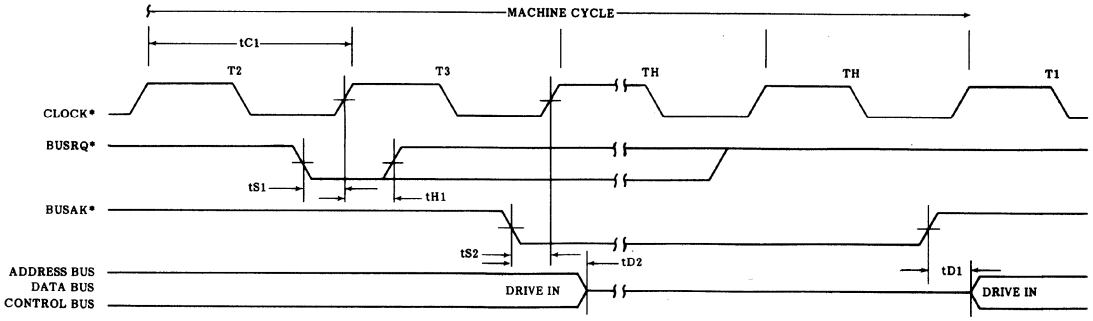
SYMBOL	PARAMETER	UNIT	6.250 MHz		6.144 MHz	
			MIN	MAX	MIN	MAX
tC1	Clock cycle time	ns		320		325
tD1	Address delay from T1 clock	ns		135		135
tD2	Data delay from WR*	ns		55		55
tH1	Address hold time	ns	100		100	
tH2	Data hold time	ns	80		85	
tS1	Address setup before write strobe	ns	640		650	
tS2	Data setup before write strobe	ns	400		410	
tW1	WR* pulse width	ns	385		390	

Figure 2-12. Write Timing: Memory Write and Output (7815)



SYMBOL	PARAMETER	UNIT	6.250 MHz		6.144 MHz	
			MIN	MAX	MIN	MAX
tC1	Clock cycle time	ns		320		325
tH1	WAITRQ* hold time after T2/TW	ns	0		0	
tS1	Address setup before WAITRQ*	ns		175		180
tS2	WAITRQ* setup before T2/TW	ns	110		110	

Figure 2-13. Wait Request Timing (7815)



SYMBOL	PARAMETER	UNIT	6.250 MHz		6.144 MHz	
			MIN	MAX	MIN	MAX
tC1	Clock cycle time	ns		320		325
tD1	Bus delay after BUSAK* high	ns		210		210
tD2	Bus delay after BUSAK* low	ns		195		200
tH1	BUSRQ* hold after start of T3	ns	0		0	
tS1	BUSRQ* setup prior to T3	ns	195		195	
tS2	BUSAK* setup prior to TH	ns	95		95	

Figure 2-14. BUS Request Timing (7815)

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

Figures 2-15 and 2-16 show the electrical specifications for the 7815. Environmental specifications are shown in figure 2-17. Figure 2-18, page 2-15, gives pinout and loading characteristics of the connection between the 7815 and the STD BUS.

			RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS	
MNEM.	PARAMETER	UNIT	MIN	TYP	MAX	MIN	MAX
VCC	Logic Supply	V	4.75	5.00	5.25	0	5.50

Figure 2-15. Electrical Specifications (7815)

			RECOMMENDED OPERATING LIMITS		
MNEM.	PARAMETER	UNIT	MIN	TYP	MAX
ICC*	VCC Supply Current	mA	—	530	815

Figure 2-16. Electrical Characteristics Over Operating Range (7815)

*ICC specification assumes memory sockets are empty (as shipped). For maximum memory currents add 110 mA (maximum) selected, 3 mA (maximum) standby per 8K by 8 static RAM (Hitachi HM6264P type), and 100 mA selected, 40 mA standby per 8K by 8 EPROM (Intel 2764 type).

			RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS	
MNEM.	PARAMETER	UNIT	MIN	TYP	MAX	MIN	MAX
—	Free Air Temp.	°C	0	+25	+65	-40	+75°C
—	Humidity, Non-condensing	%RH	5	—	95	5	95

Figure 2-17. Environmental Specifications (7815)

POWER-ON AND PUSHBUTTON RESET

Power-on reset holds the SYSRESET* line low and releases it 60 ms (maximum) after the VCC reaches 4.75V. The PBRESET* is debounced approximately 20 ms, and produces a 65 ms (maximum) SYSRESET* pulse.

CABLING

The J1 Segment connector can use a Pro-Log RC704-1 or RC704-2 cable. These cables are one (RC704-1) or two (RC704-2) feet of twisted-pair wires with a 2-pin connector on each end. These cables mate to the card responding to Segment (e.g., the Pro-Log 7704 memory card).

MECHANICAL SPECIFICATIONS

The 7815 meets all general mechanical specifications of the STD BUS. Refer to the STD Specification and Practice for outline dimensions.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	IN		+5V	1		IN	+5V
4	IN		GROUND	3		IN	GROUND
6			-5V	5			-5V
8	1	55	D7	7	55	1	D3
10	1	55	D6	9	55	1	D2
12	1	55	D5	11	55	1	D1
14	1	55	D4	13	55	1	D0
16	1	55	A15	15	55	1	A7
18	1	55	A14	17	55	1	A6
20	1	55	A13	19	55	1	A5
22	1	55	A12	21	55	1	A4
24	1	55	A11	23	55	1	A3
26	1	55	A10	25	55	1	A2
28	1	55	A9	27	55	1	A1
30	1	55	A8	29	55	1	A0
32	1	55	RD*	31	55	1	WR*
34	1	55	MEMRQ*	33	55		IORQ*
36		55	MEMEX	35	OUT		IOEXP
38		55	MCSYNC*	37			REFRESH*
40		55	STATUS 0*	39	55		STATUS 1*
42	3		BUSRQ*	41	55		BUSAK*
44	3		INTRQ*	43	55		INTAK*
46	3		NMIRQ*	45		3	WAITRQ*
48	A		PBRESET*	47	55		SYSRESET*
50			CNTRL*	49	55		CLOCK*
52	IN		PCI	51	OUT		PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

A Switch Input
* Designates active low-level logic

Figure 2-18. STD BUS Edge Connector Pin List (7815)

INTRODUCTION

This section describes the theory of operation for the 7815 power-on/pushbutton reset circuit and memory expansion (MEMEX and Segment) control.

POWER-ON AND PUSHBUTTON RESET CIRCUIT

The 7815 reset circuit consists mainly of two voltage comparators. The first comparator turns on only when the power supply reaches a voltage in the operating range. After the first comparator turns on, indicating a valid operating voltage, RESET* must be held low until the clock oscillator functions. This is accomplished by having the first comparator charge an RC network, which inputs to the second voltage comparator. The second comparator turns on and sets RESET* high after an RC time constant equal to the oscillator startup time (60 ms maximum).

Figure 3-1 shows the 7815 reset circuit.

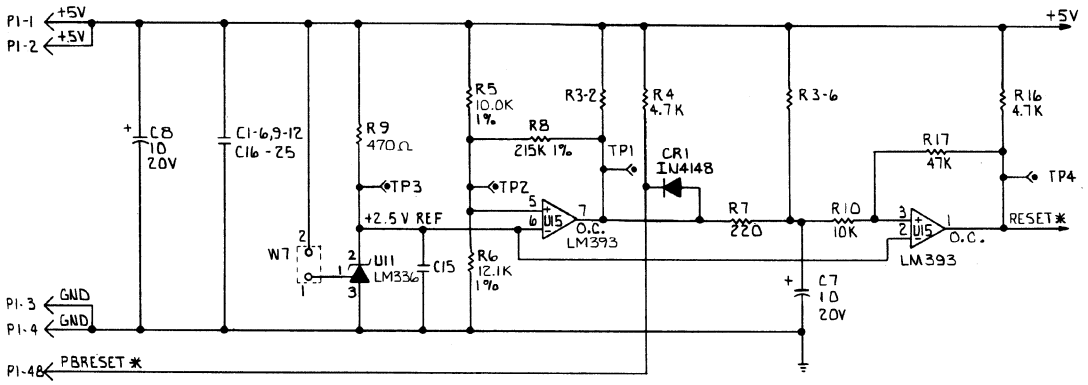


Figure 3-1. Reset Circuit (7815)
FOR REFERENCE ONLY

R9 and U11 generate a reference voltage for the two comparators. R5 and R6 form a voltage divider for the supply voltage. R3-6 (4.7K) and C7 form the oscillator startup RC time constant network. R8 and R17 provide hysteresis for the voltage comparators to prevent oscillations.

The remainder of the reset circuit is associated with a pushbutton reset. The pushbutton input is debounced by a circuit consisting of a comparator (U15) and an RC network (R4 and C7). The PBRESET* is effectively wire-ORed with the power-on reset signal through CR1 and becomes the RESET* signal.

MEMEX AND SEGMENT CONTROL

Both MEMEX and Segment allow expansion of the system memory capacity. MEMEX is implemented through the STD BUS and Segment is implemented through the user connector J1. Since MEMEX is on the STD BUS, it is a signal that can be used by any card. Segment, on the other hand, is only used when it is connected by cable to a card that responds to Segment. Otherwise, MEMEX and Segment are the same. MEMEX affects the entire system, since it is an STD BUS signal. Segment affects only the card to which it is connected. In the following description of the theory of operation MEMEX is used, but the theory holds true for Segment as well.

MEMEX allows the user to select between two banks of memory. To use MEMEX, the program writes to the on-card port. MEMEX uses bit D0 of the port, and Segment uses bit D1. Writing to the port immediately affects the memory expansion line polarities.

Figure 3-2 shows a system with 96K of memory. The on-card memory consists of four 8K by 8 ROMs residing at addresses 0000-7FFF. This memory is permanently enabled and can be addressed whether MEMEX is high or low. The other 64K block is RAM and is divided into two 32K banks on separate cards. Both banks reside at addresses 8000-FFFF. One bank is enabled by MEMEX low and the other is enabled by MEMEX high. With this scheme, the main part of the software driver can reside in the on-card memory at addresses 0000-7FFF. This main program uses MEMEX to switch back and forth between the two banks of RAM.

Figure 3-3, page 3-4, shows a system with 128K of memory split into two 64K banks. Both banks reside at addresses 0000-FFFF. The on-card memory sockets of the 7815 are not used, and are disabled by removing the associated jumpers (see figure 2-3, page 2-3). Therefore, MEMEX does not affect the on-card memory at all. The software drivers for this system must be located in both banks of memory, because once control is switched to the other bank there is no way to get back without the driver. For example, if the system driver program in the primary bank changed MEMEX high with no driver in the secondary bank, there would be no instructions to send MEMEX low and send the processor back to the primary bank. There must be some kind of memory bank control in both banks.

When switching MEMEX, the address of the present memory location does not change. For example, in the system shown in figure 3-2, if the program counter that holds the address of the next instruction were pointing at 4000 in the primary memory bank and MEMEX were switched high, the program counter would still be pointing to 4000, but in the secondary memory bank. Once at that point any instruction may be executed, but it must be located at address 4000. To use MEMEX you must know the current location in both banks of memory so control is not lost switching between banks.

Section 4 contains a software example of MEMEX Control.

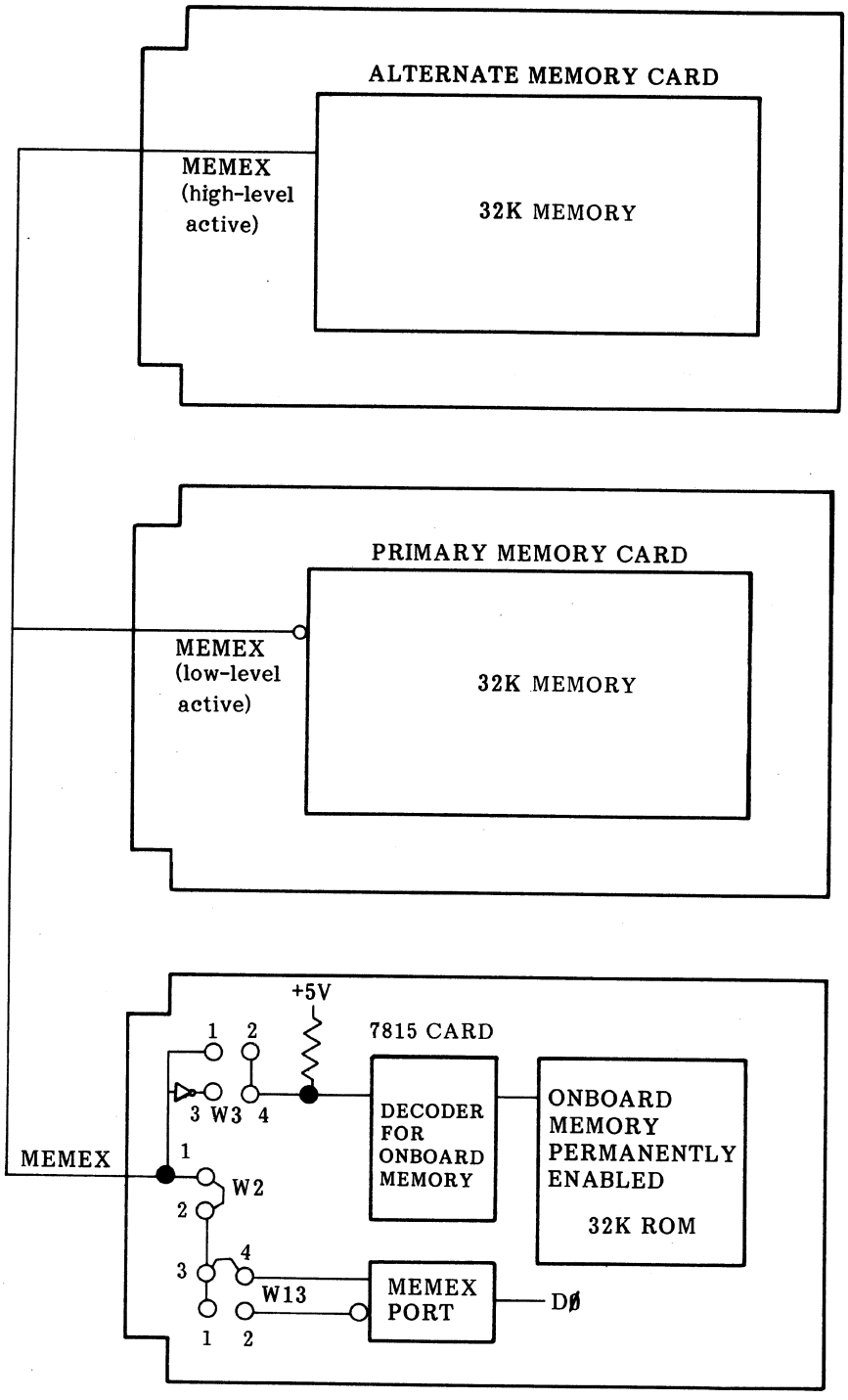


Figure 3-2. Example of MEMEX for Selecting Between Two Banks of Memory in a 96K Memory System.

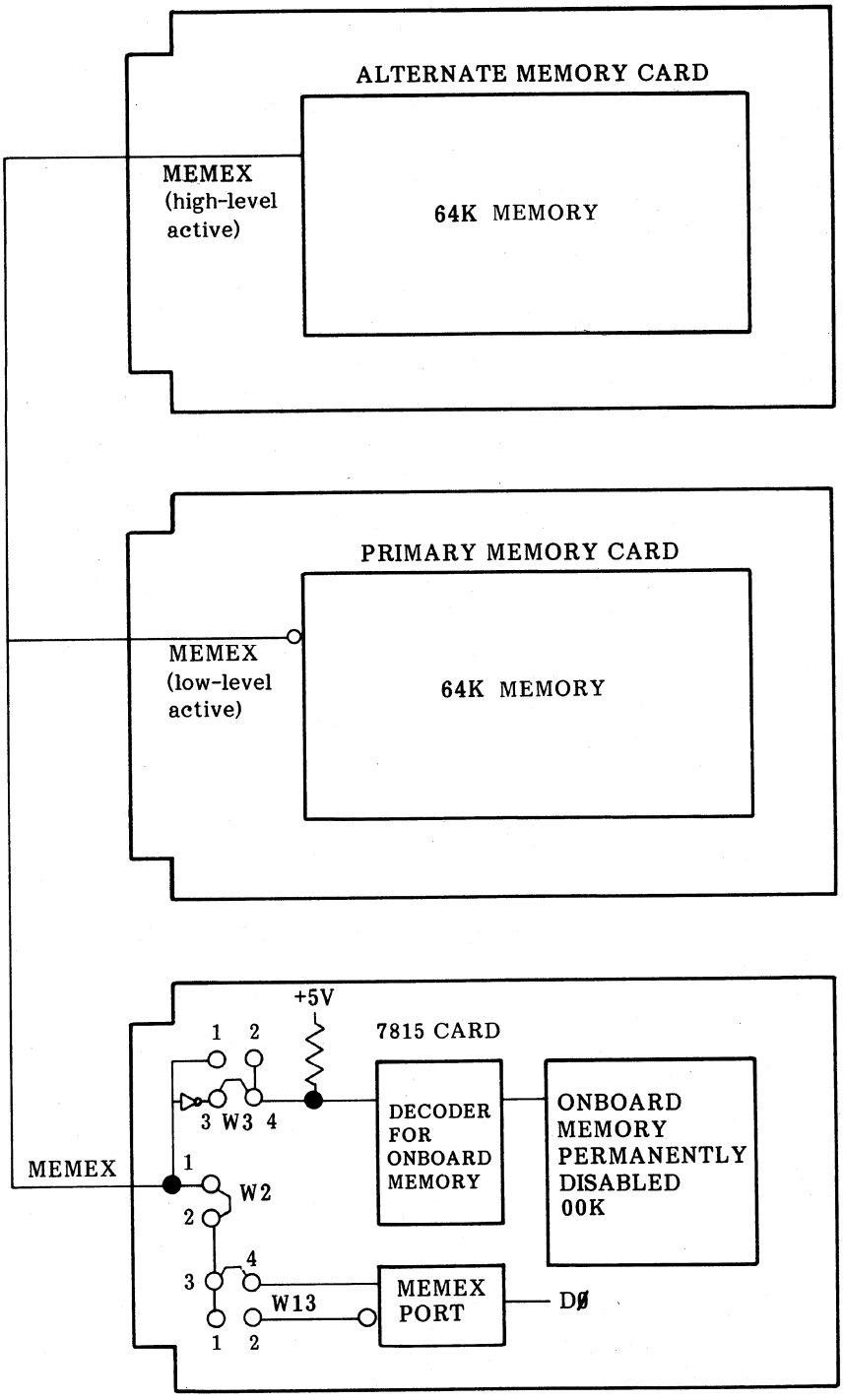


Figure 3-3. Example of MEMEX for Selecting Between Two Banks of Memory in a 128K System

MEMEX CONTROL SOFTWARE EXAMPLE

This section contains an example of a memory-management application using MEMEX. It explains how MEMEX can be used to enable one of two banks of memory mapped at the same address. The example assumes that the user has decided which bank to select as a requirement of the main program. Thus, the program enters one of the two MEMEX Control Subroutines.

Software Functional Description

Executing either subroutine, the MEMEX I/O port is enabled and MEMEX is activated. The polarity of the active state of MEMEX is determined by the jumper positions of W13. Next in sequence, the address at which the program executes in bank 0 or 1 is loaded into registers H,L and stored on the stack. Registers H,L are then loaded with the return address. The "XCPN HL,(SP)" instruction exchanges the contents of the current 2-byte location (pointed to by the stack register) with the return address currently loaded into registers H,L. Using the "JPN (HL)" instruction, the program is immediately executed in either bank 0 or bank 1 memory. Upon completion of the subroutine(s), program control returns to the user's main program.

Hardware Functional Description

In addition to the 7815 onboard memory, two 7704 memory cards comprise the memory system for this example. Figure 4-1 is a diagram of the 96K memory system. The 7815 has 32K of permanently enabled memory which disregards MEMEX. The MEMEX control software resides here. The 7815 onboard memory is mapped from 0000 to 7FFF (the first 32K in a 64K map). See figure 2-4, page 2-4, for the 7815 memory mapping with jumper W10.

Each 7704 is mapped from 8000 to FFFF (32K each). One 7704 is assigned as bank 0 and the other as bank 1. Bank 0 is enabled when MEMEX is low and bank 1 when MEMEX is high. Refer to the 7704 User's Manual, figure 2-6, page 2-6, for 7704 memory mapping. See figure 2-4, page 2-3, to configure the 7704 for MEMEX.

The 7815 has an onboard MEMEX/Segment port which can be addressed as either port FE or port 7F. See section 2, figure 2-9, page 2-7, to configure the port address. This example assumes that the onboard port is mapped at FE.

The 7815 onboard memory is made independent of MEMEX by removing the jumper from W3. This makes the 7815 onboard memory permanently enabled. At power-up, the MEMEX port is low with W13 in the as-shipped position (pins 3 and 4 shorted).

See section 3, page 3-2, for a detailed description of MEMEX and its control.

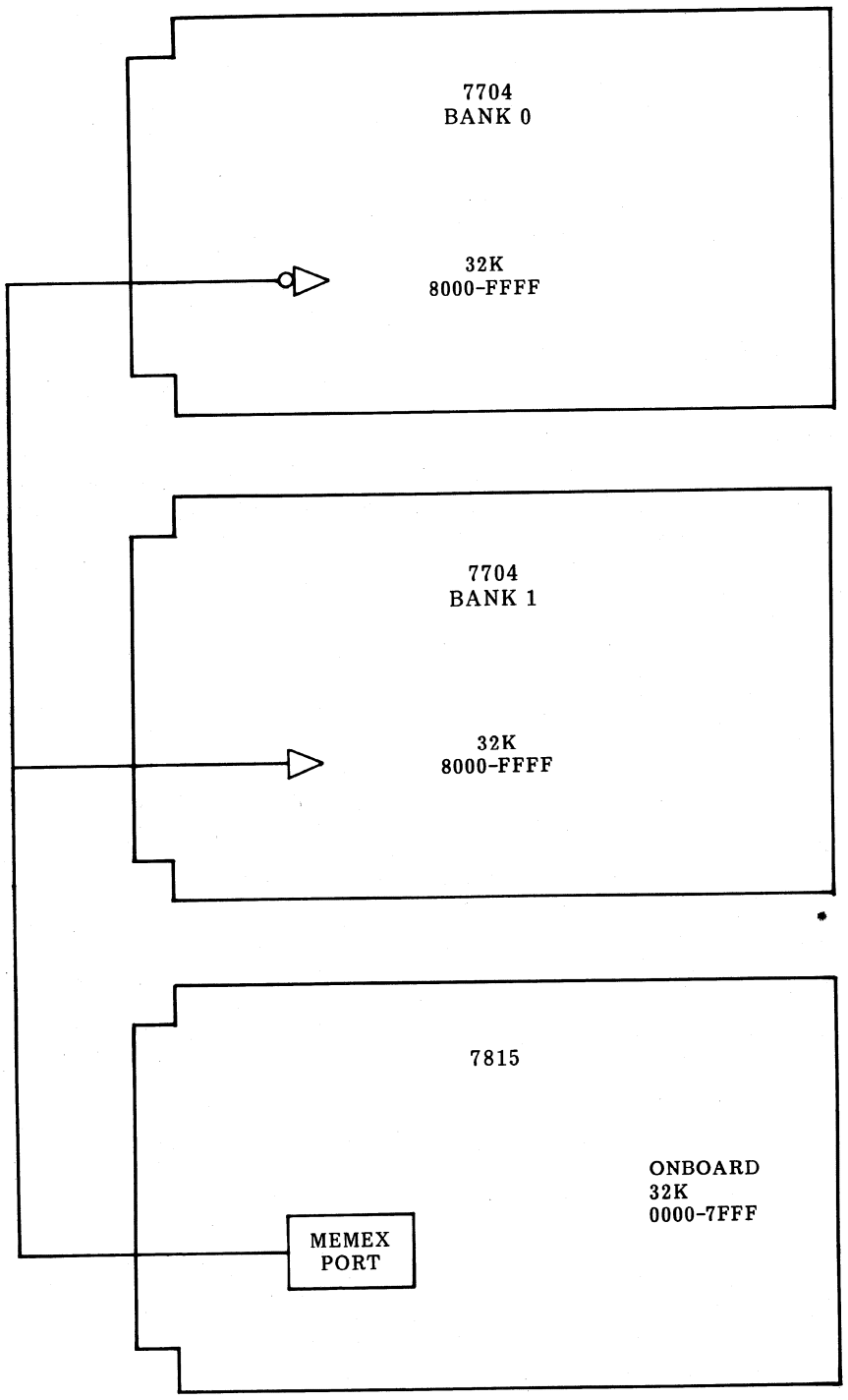


Figure 4-1. MEMEX Control Software Example Diagram (7815)

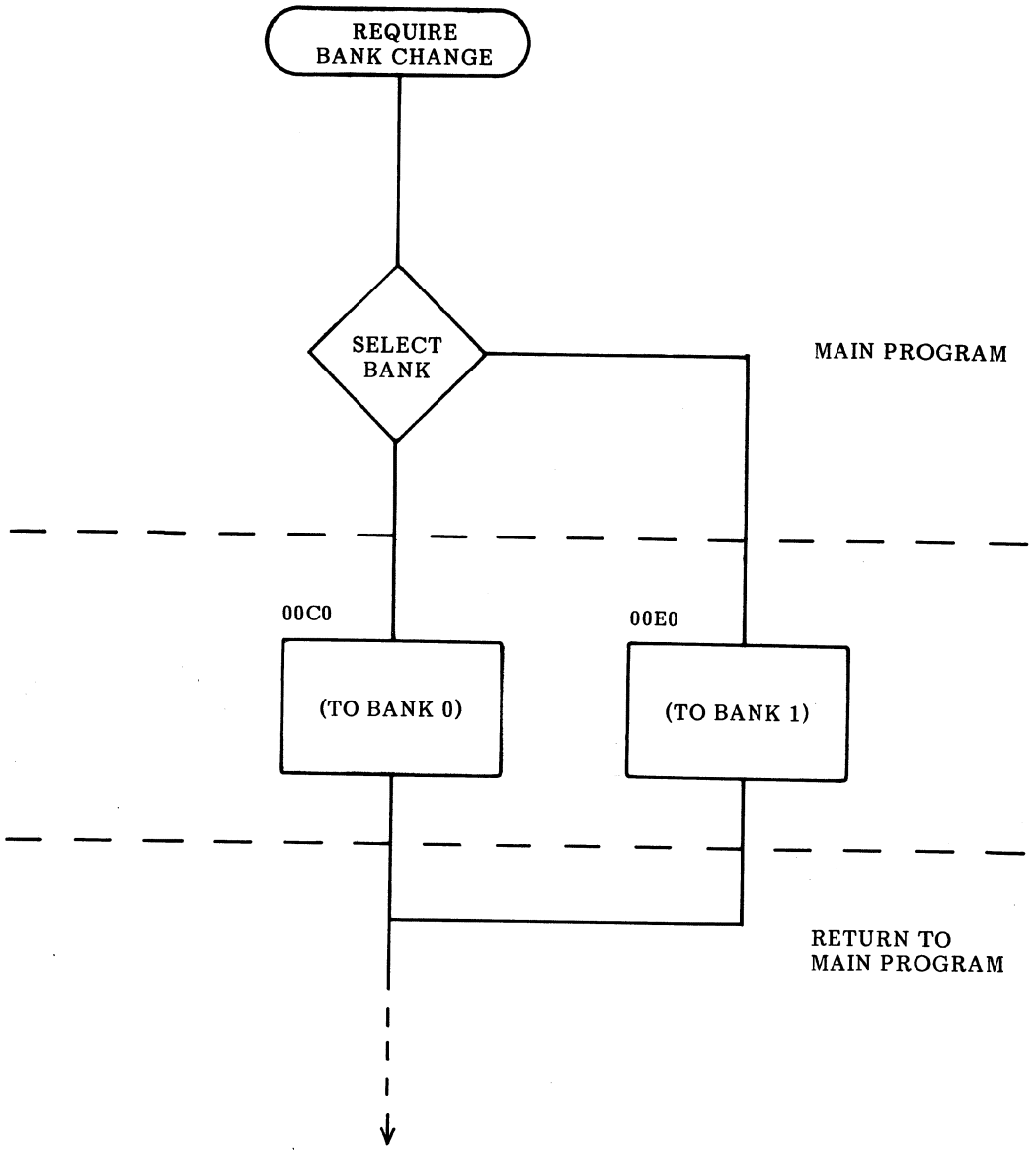


Figure 4-2. MEMEX Control Software Example Flowchart

ADRdata	LABEL	INSTR	MODIFIER	COMMENTS
00C0 3E	[GO TO BANK 0]	LDAI		ENABLE BANK 0 MEMORY
C1 00		----	00	SET MEMEX LOW
C2 D3		OPA		
C3 FE		----	FE	7815 MEMEX PORT ADDRESS
C4 21		LDPI	HL	STORE MEMORY LOCATION TO
C5 20		----	8020	AEXECUTE FROM IN BANK 0
C6 80		----		
C7 E5		PSP	HL	SAVE NEW ADDRESS ON THE STACK
C8 21		LDPI	HL	LOAD RETURN ADDRESS
C9 C0		----	00C0	
CA 00		----		
CB E3		XCPN	HL,(SP)	JUMP TO SUBROUTINE POINTED TO
CC E9		JPN	(HL)	BY REGISTERS H,L
CD C9	----------	RTS	UN	RETURN TO MAIN PROGRAM
CE FF				
CF FF				
00D0 FF				
D1 FF				
D2 FF				
D3 FF				
D4 FF				
D5 FF				
D6 FF				
D7 FF				
D8 FF				
D9 FF				
DA FF				
DB FF				
DC FF				
DD FF				
DE FF				
DF FF				
00E0 3E	[GO TO BANK 1]	LDAI		ENABLE BANK 1 MEMORY
E1 01		----	01	SET MEMEX HIGH
E2 D3		OPA		
E3 FE		----	FE	7815 MEMEX PORT ADDRESS
E4 21		LDPI	HL	STORE MEMORY LOCATION TO
E5 20		----	8020	EXECUTE FROM IN BANK 1
E6 80		----		
E7 E5		PSP	HL	SAVE NEW ADDRESS ON THE STACK
E8 21		LDPI	HL	LOAD RETURN ADDRESS
E9 ED		----	00ED	
EA 00		----		
EB E3		XCPN	HL,(SP)	JUMP TO SUBROUTINE POINTED TO
EC E9		JPN	(HL)	BY REGISTERS H,L
ED C9	----------	RTS	UN	RETURN TO MAIN PROGRAM
EE FF				
EF FF				
00F0 FF				
F1 FF				
F2 FF				
F3 FF				
F4 FF				
F5 FF				
F6 FF				
F7 FF				
F8 FF				
F9 FF				
FA FF				
FB FF				
FC FF				
FD FF				
FE FF				
FF FF				

Figure 4-3. MEMEX Control Software Example Program Listing

REFERENCE DRAWINGS

The schematic (figures 5-1 and 5-2) and assembly drawing (figure 5-3) in the following pages are included in this manual FOR REFERENCE USE ONLY. Because improvements may have been made after this manual was published, they may differ in some respects from the card and documentation that the user received from Pro-Log.

The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

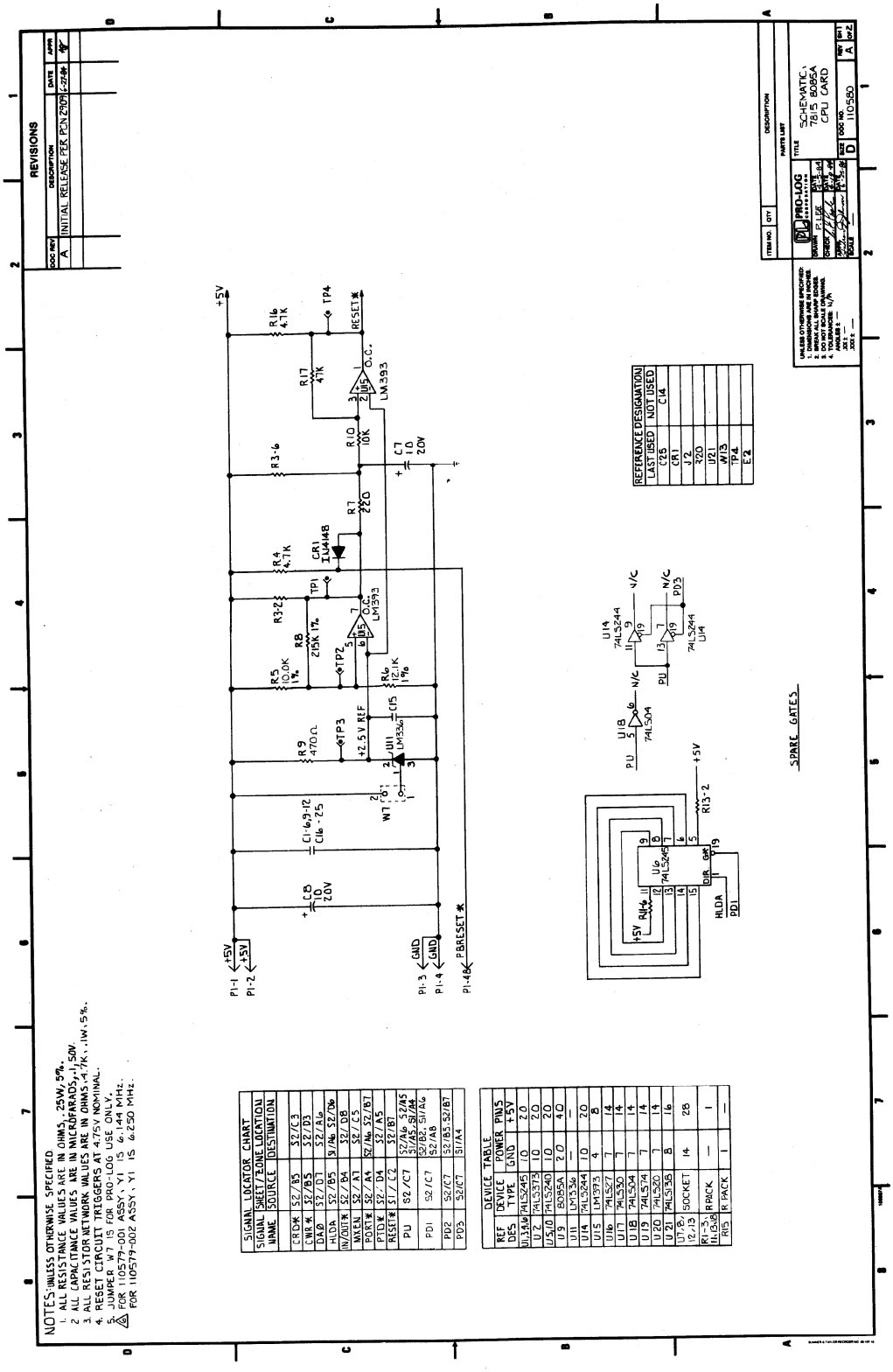

REVISIONS
A INITIAL RELEASE PER PCN 2909L-2284
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS, .25W, 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 1, 50V.
3. ALL RESISTOR NETWORK VALUES ARE IN OHMS 4.7K, 1W, 5%.
4. RESET CIRCUIT TRIGGERS AT 4.75V NOMINAL.
5. JUMPER W7 IS FOR PRO-LOG USE ONLY.
FOR 110579-001 ASSY, Y1 IS 6.144 MHz.
FOR 110579-002 ASSY, Y1 IS 6.250 MHz.
SIGNAL LOCATOR CHART
DEVICE TABLE
REFERENCE DESIGNATION
SPARE GATES
PRO-LOG
SCHEMATIC, 7815 8085A CPU CARD
DOC NO 110580
SIZE D
REV A

Figure 5-1. 7815 Schematic (sheet 1)
(FOR REFERENCE ONLY)

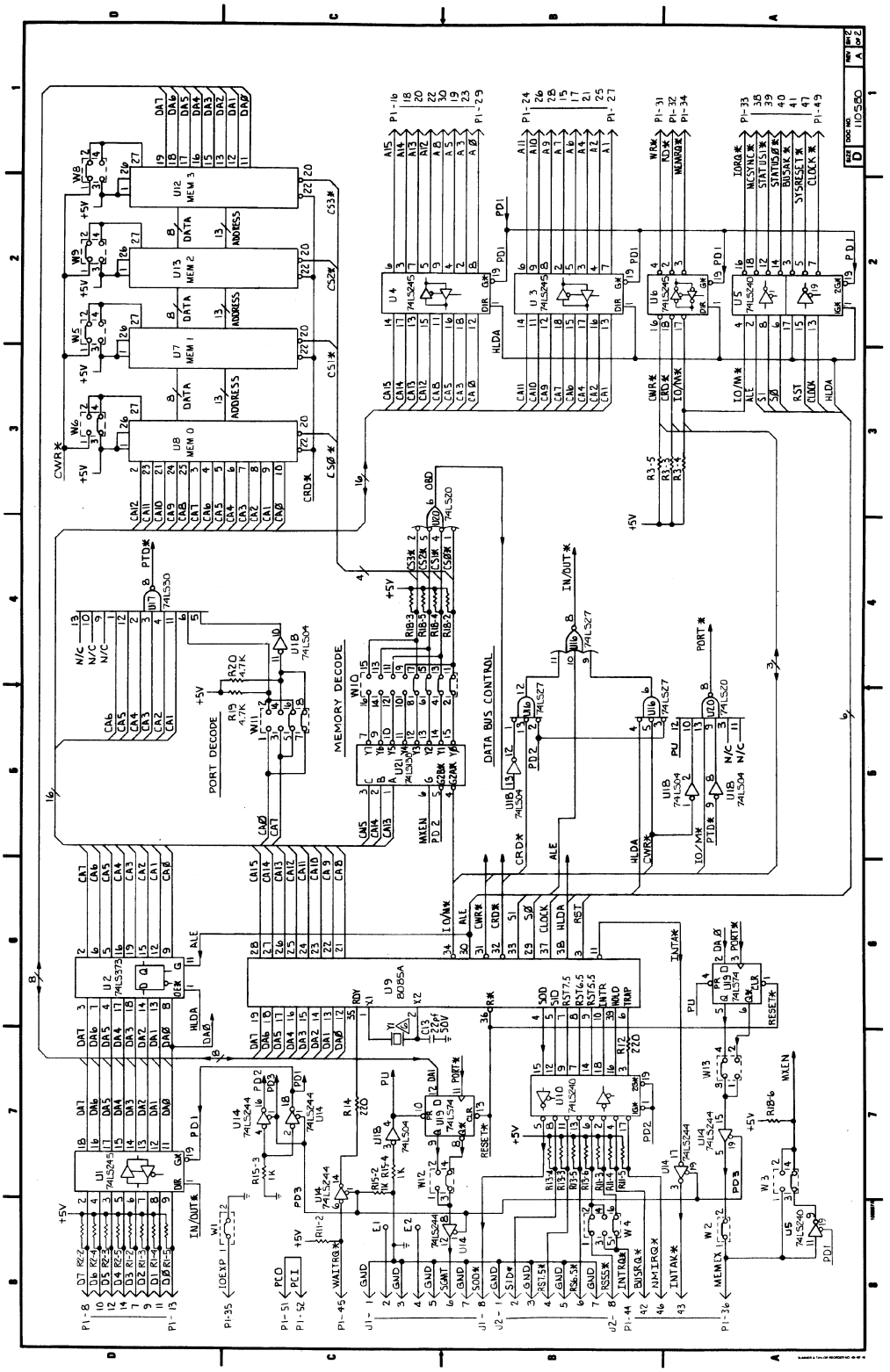


Figure 5-2. 7815 Schematic (Sheet 2)
(FOR REFERENCE ONLY)

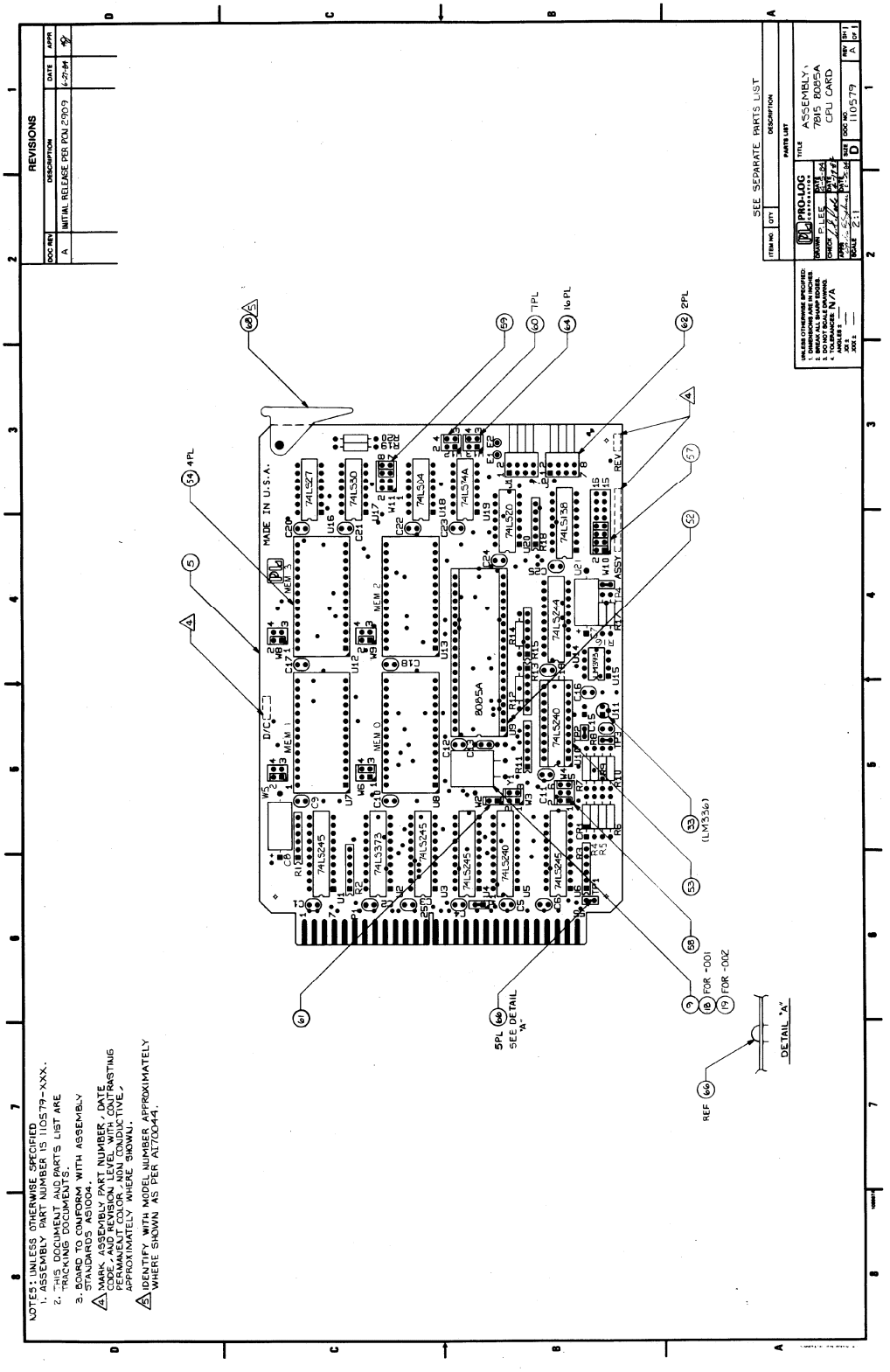


Figure 5-3. 7815 Assembly Drawing (FOR REFERENCE ONLY)

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call CUSTOMER SERVICE at (408) 372-4593 (in California) or (800) 538-9570 (outside of California) 7 AM to 3 PM PST.

2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.

3. Please be sure to enclose a packing slip with the CRO number, the equipment serial number if applicable, and the reason for return. Also enclose the name and telephone number of the person we should contact (preferably the user).

4. Package the equipment in a solid cardboard box secured with packing material.

CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, CA 93940
   Reference CRO #_____.

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

LIMITED WARRANTY:

Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. This liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair, or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller of the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

Cut Here

FOLD

FOLD

PRO-LOG® CORPORATION

Yes, I'm interested in Pro-Log.
Please send me more information about your:

- ☐ 7000 Series STD BUS Cards
- ☐ STD BUS Packaging Solutions
- ☐ STD BUS Subsystem
- ☐ STD BUS Systems
- ☐ Designer Software
- ☐ Design Courses and Seminars
- ☐ Programmer Product Line
- ☐ Other _____

- ☐ I am currently using Pro-Log equipment.
- ☐ Add my name to your mailing list.
- ☐ Please have a Sales Representative contact me.

Reader Comments: _____

Name _____ City _____
Company _____ State _____ Zip _____
Address _____ Telephone _____

PLACE
POSTAGE
HERE

PRO-LOG®
CORPORATION
2411 GARDEN ROAD
MONTEREY, CA 93940

Attn: Literature Department

Notes

Notes